ATTORNEY DOCKET NO. 00-C-015 (STMI01-00015) U.S. SERIAL NO. 09/656,985 PATENT

PENDING CLAIMS:

1	1. (unchanged) A method of forming a linear photosensor array, comprising:
2	forming a plurality of integrated circuits each including a linear array of photosensors within
3	a portion of the integrated circuit remaining exposed after packaging and a plurality of conductive
4	leads adapted for soldering to a circuit board;
5	mounting the integrated circuits with the portions containing the photosensors in alignment
6	on a circuit board; and
7	soldering at least some of the leads for each integrated circuit to the circuit board.

1	2. (unchanged) The method of claim 1, wherein the step of forming a plurality of integrated circuits
2	each including a linear array of photosensors within a portion of the integrated circuit remaining
3	exposed after packaging and a plurality of conductive leads adapted for soldering to a circuit board
4	further comprises:
5	packaging each of the plurality of integrated circuit packages by:
6	affixing an integrated circuit die to a lead frame;
7	connecting the integrated circuit die to selected portions of the lead frame with bond
8	wires; and
9	encapsulating a portion of the lead frame and the integrated circuit die except for the
10	exposed region, wherein the exposed region of the integrated circuit die remains exposed to
11	external ambient light.

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3. (unchanged) The method of claim 2, wherein the step of encapsulating a portion of the lead frame
and the integrated circuit die except for the exposed region, wherein the exposed region of the
integrated circuit die remains exposed to external ambient light further comprises:

after affixing the integrated circuit die to the lead frame and connecting the bond wires, mounting the lead frame with the integrated circuit die and bond wires in a mold with a portion of the mold in contact with the exposed region of the integrated circuit die to prevent encapsulating material from adhering to the exposed region of the integrated circuit die.

4. (unchanged) The method of claim 3, wherein the step of mounting the lead frame with the integrated circuit die and bond wires in a mold with a portion of the mold in contact with the exposed region of the integrated circuit die to prevent encapsulating material from adhering to the exposed region of the integrated circuit die further comprises:

mounting the lead frame with the integrated circuit die and bond wires in a mold having a sloped surface adjacent to the portion of the mold contacting the exposed region of the integrated circuit die, wherein the sloped surface forms one surface of a mold cavity receiving the bond wires when the lead frame with the integrated circuit die is mounted in the mold.

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5. (unchanged) The method of claim 1, wherein the step of forming a plurality of integrated circuits		
each including a linear array of photosensors within a portion of the integrated circuit remaining		
exposed after packaging and a plurality of conductive leads adapted for soldering to a circuit board		
further comprises:		
mounting a plurality of integrated circuit die on a lead frame strip with a separation between		

the mounted integrated circuit die approximately equal to a kerf width for a singulation saw to be used in separating the packaged integrated circuits.

- 6. (unchanged) The method of claim 1, wherein the step of mounting the integrated circuits with the portions containing the photosensors in alignment on a circuit board further comprises:
- packaging the integrated circuits with the portion containing the photosensors exposed; and mounting adjacent packaged integrated circuits in contact with each other.
 - 7. (unchanged) The method of claim 1, wherein the step of soldering at least some of the leads for each integrated circuit to the circuit board further comprises:
 - soldering only leads on one side of each integrated circuit to the circuit board, leaving leads on an other side of the packaged integrated circuits in floating contact with conductive structures on the circuit board to facilitate adjustment and removal of integrated circuits.